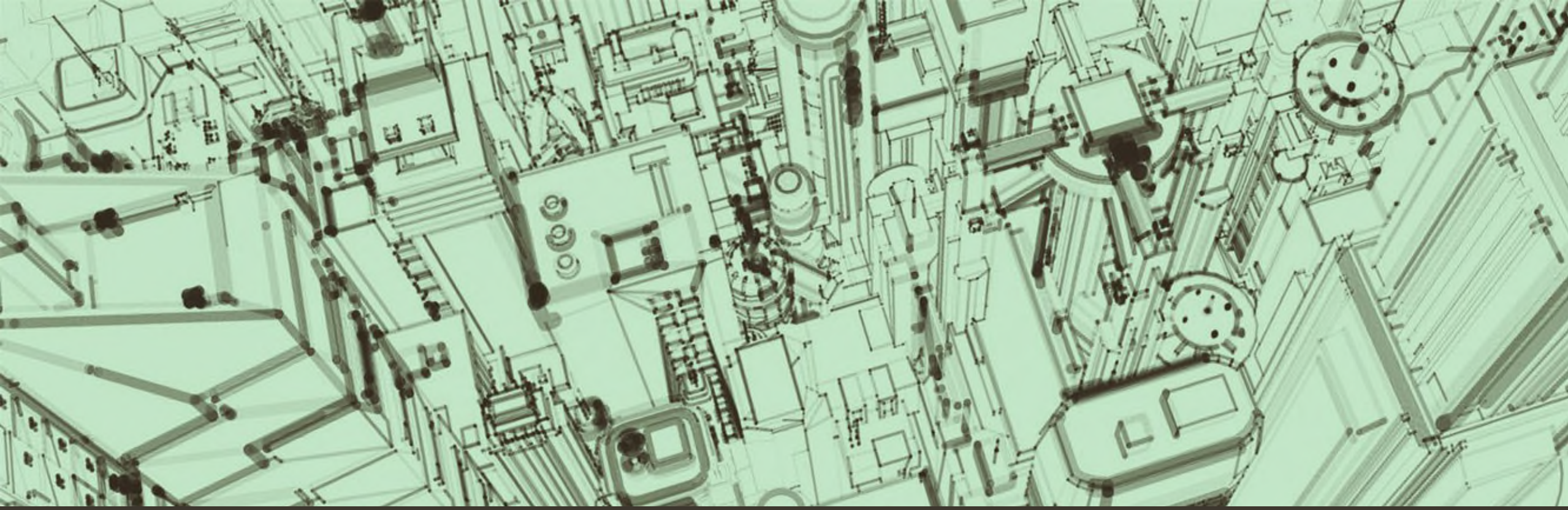

Review of TCAD DTCO FLOW

Francis Benistant
December 16th 2021

TCAD DTCO FLOW

- Contents

  - **TCAD Company Status**
  - TCAD DTCO FLOW
  - Synopsys DTCO FLOW
  - Silvaco DTCO FLOW
  - GTS DTCO FLOW
  - Future of TCAD DTCO Flow

TCAD Company History

- 80s: TMA - Stanford University code (2D Tsuprem4 & Medici)
- 90s: SILVACO - Stanford University code (2D SSsuprem4 & Atlas)
- 90s: ISE - University of Zurich code (3D Dessis) & DDR Berlin Technical Institute code (2D DIOS)
- 1997: Avant! Acquires TMA - Taurus 3D Process & Device – First code produced by TCAD company (replaced by Sentaurus tools now)
- 2001: Synopsys acquires Avant!
- 2004: Synopsys acquires ISE
- 2006: TCAD_International founded in Japan from Selete spinoff
- 2008: GTS founded from University of Vienna spinoff
- 2008: QuantumWise founded (Ab-Initio materials simulation)
- 2009: Samsung acquires TCAD_International
- 2010: GSS founded from University of Glasgow spinoff
- 2016: Synopsys acquires GSS
- 2017: Synopsys acquires QuantumWise (became Quantum ATK)

TCAD Company Status

In 2021: Only 3 independent companies exist in TCAD
(TCAD = Technology Computer-Aided Design)

- Synopsys largest market share in TCAD (Avant! – ISE – GSS – QuantumWise tools) – positioned on Advanced Nodes – based in US
- Silvaco second market share in TCAD – positioned on High Voltage Nodes and Optoelectronic – based in EU (France), UK and US
- GTS third market share in TCAD – positioned on path finding for Advanced Logic & Memory Nodes – based in EU (Austria)

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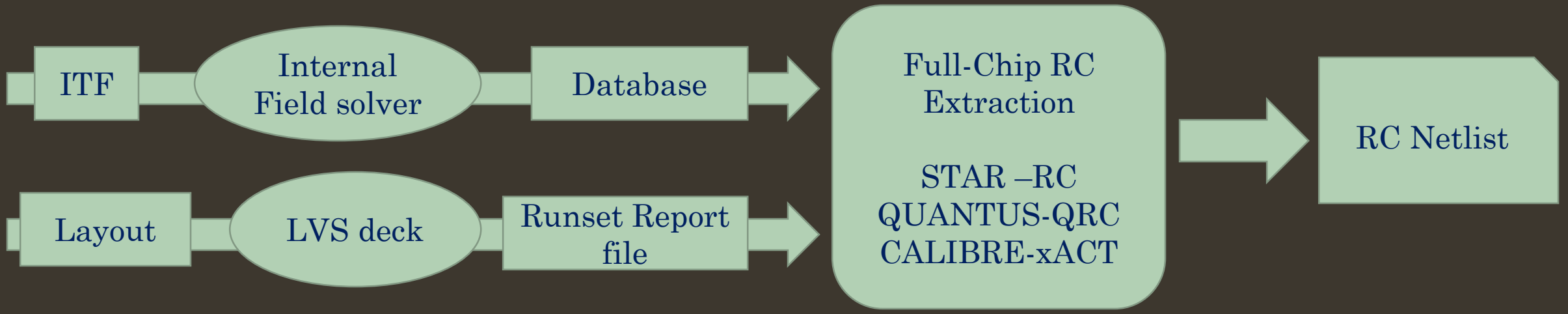
TCAD DTCO FLOW

- TCAD DTCO Flow alternative when PDK not available / no LVS deck
- TCAD DTCO Flow does not require the ITF files for PEX extraction
- ITF (Interconnect Technology File) is part of PDK as a cross-section of the process and interconnection (layer thickness, dielectric constant, resistivity, …), is made by the Foundries, and is combined with the layout for parasitic extraction (PEX)
- ITF files are encrypted in the PDK
- Typically, TCAD DTCO Flow is used for path-finding or on-going technology development
- TCAD DTCO Flow is an alternative to the rule-based EDA flow when no PDK exists

TCAD DTCO FLOW

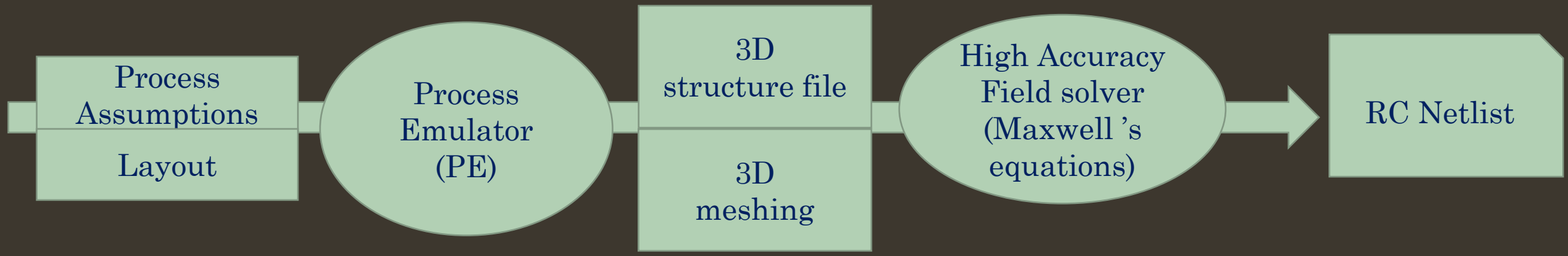
- EDA rule-based PEX Flow for post-layout parasitic extraction:
  - Technology layer file found in the Foundry PDK is the Interconnect Technology Format (ITF), or equivalent, file
  - A set of primitive structures and the ITF files are input to the internal field solver
  - This solver generates a process characterization database file (2D – 2.5D R-C library)
  - Full-chip RC extraction tools read in the circuit layout file, and through pattern matching techniques extract the parasitics



➢ Since this flow is based on database (look-up tables or macro equations) to extract the PEX netlist it requires calibration using a very accurate Field Solver (like Raphael) on specific standard library cells

TCAD DTCO FLOW

- TCAD PEX extraction Flow :
  - Process Emulator (PE) generates very quickly 3D standard cell structures based on new layouts / Process Assumptions (PAs)
  - Field solver performs RC parasitic extraction w/o ITF files at the early stage of a technology development using 3D structures
  - Advantages : no ITF is needed – no LVS/PDK needed – PAs testing w/o silicon for cost saving and faster turnaround time for technology development



- This flow is based on Field Solver (usually Raphael or equivalent) to extract the PEX netlist
- It requires meshing of 3D TCAD structure to get accurate RC extraction

Overview of RC extraction flows

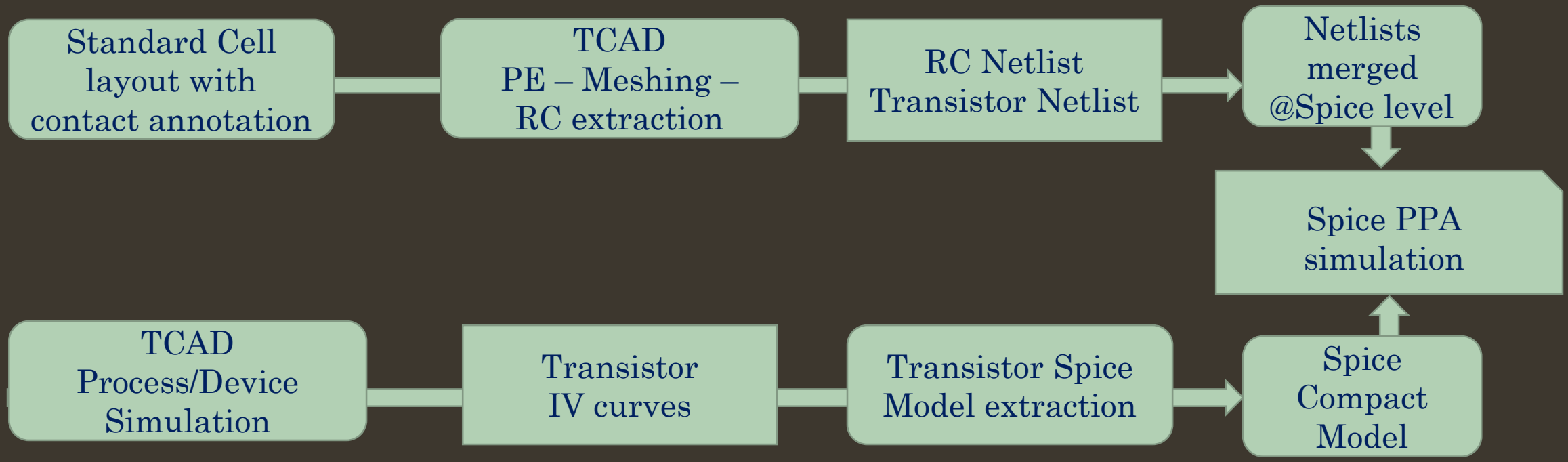
(based on Synopsys Tools as Raphael is the reference Golden Field Solver)

Flow in Historical sequence	Tools	3D Meshing	Flow Application
GDS + ITF + RC3	Raphael gds2ra (GDS+ITF) - Raphael RC3	Yes	Field solver PEX (reference for EDA PEX)
GDS + ITF + StarRC	ICV (LVS) – StarRC (PEX)	No	EDA rule-based Flow
GDS + PE + RCX	PE - Snmesh - Raphael RCX	Yes	TCAD based RC Flow

- PE: Process Explorer (Process Emulator toll) for 3D structure generation based on layout
- RC3: 3D Raphael Field Solver based on 3D structure generated from ITF files and Layout (limited to rectangular mesh and shapes)
- RCX: 3D Raphael Field solver reading TCAD 3D files from Sentaurus Process/Interconnect tools (more complex & accurate 3D structure shape using tetrahedral mesh from Snmesh tool) - PE outputs boundary file re-meshed in Snmesh

TCAD DTCO FLOW

- PEX extraction is needed for TCAD DTCO but not enough
- PEX netlist needs to be linked to circuit (transistor) netlist (e.g. RO – Inverter – SRAM cell)
- Transistor netlist is extracted using TCAD 3D Field solver sub-routine (based on connectivity)
- PEX & Circuit netlists are extracted together or merged at spice level (share the same contacts as annotated on layout)
- Spice transistor model is extracted from TCAD
- Variability can be included in the spice model based on direct Monte Carlo or post-processing IFM (Impedance Field method) methods



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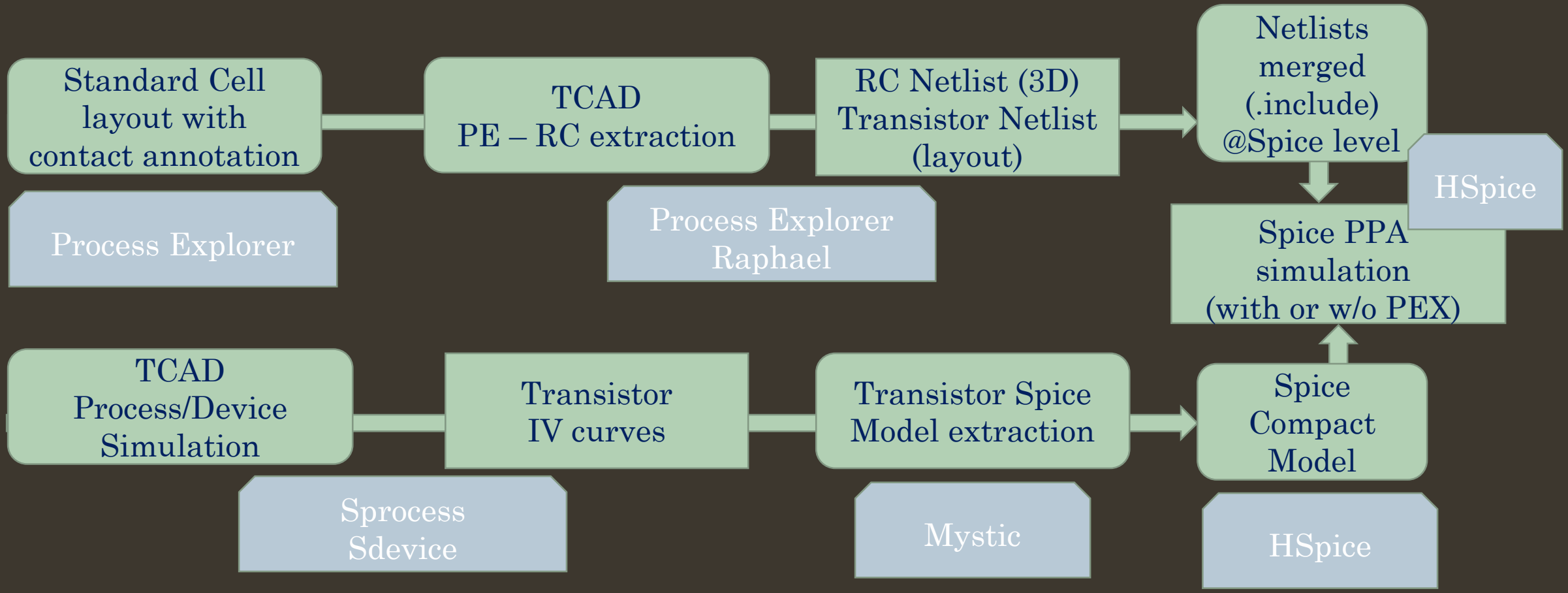
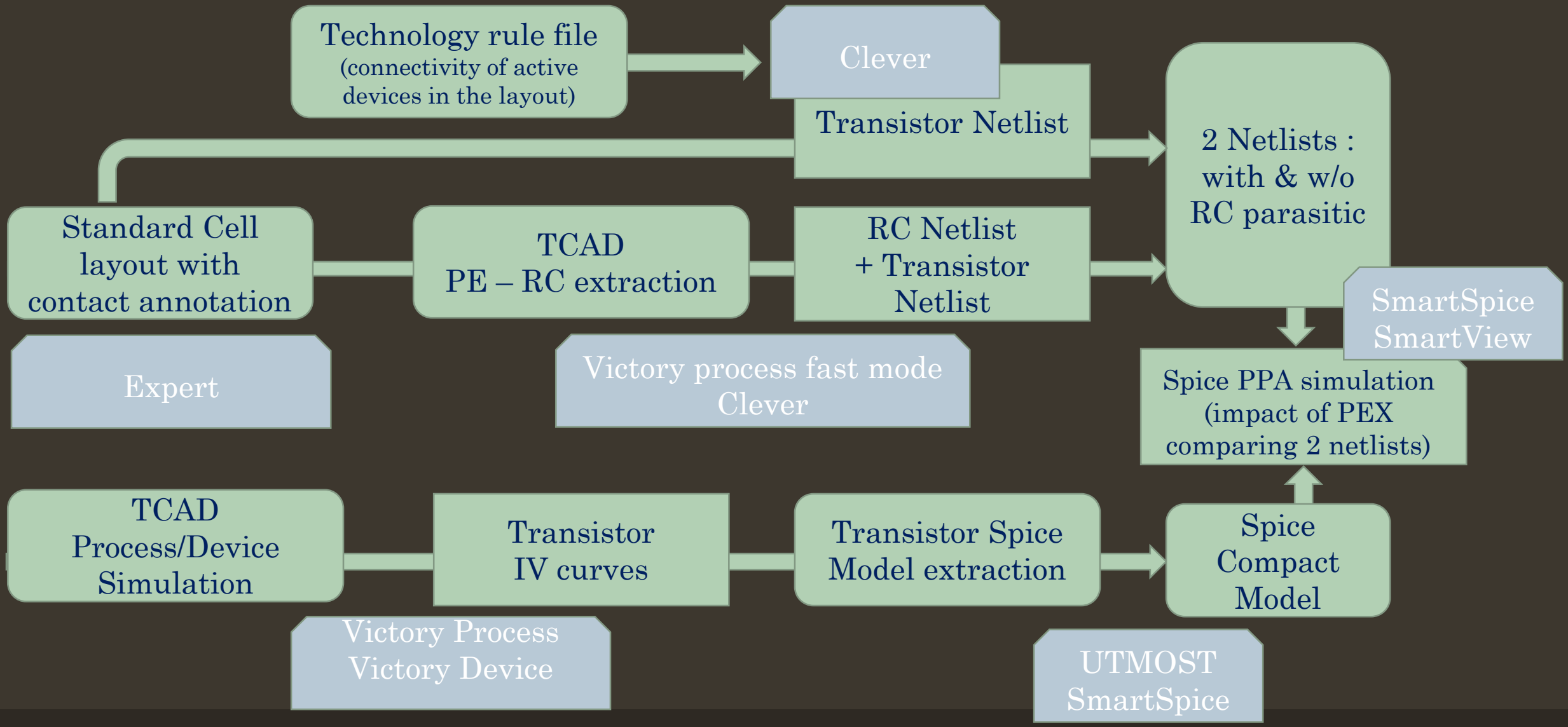
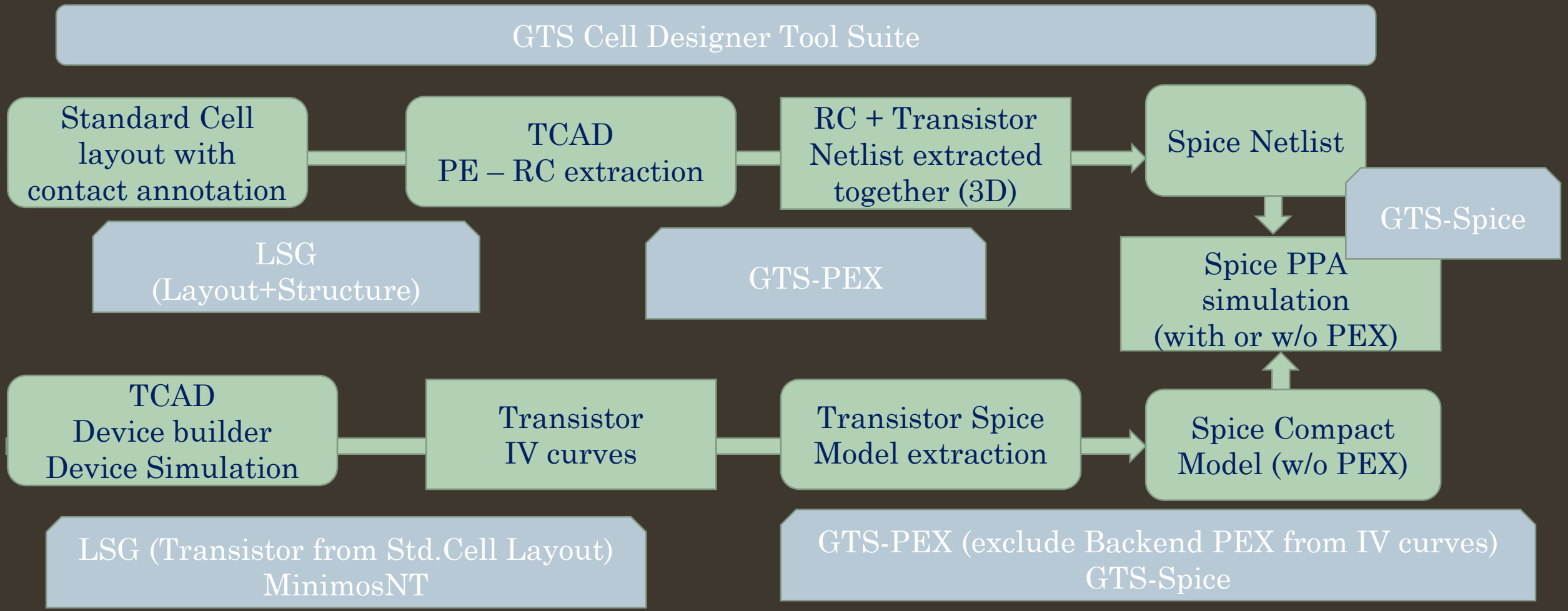
TCAD DTCO FLOW : Synopsys (Standard Cell)



TCAD DTCO FLOW : Silvaco (Standard Cell)



TCAD DTCO FLOW : GTS (Standard Cell)



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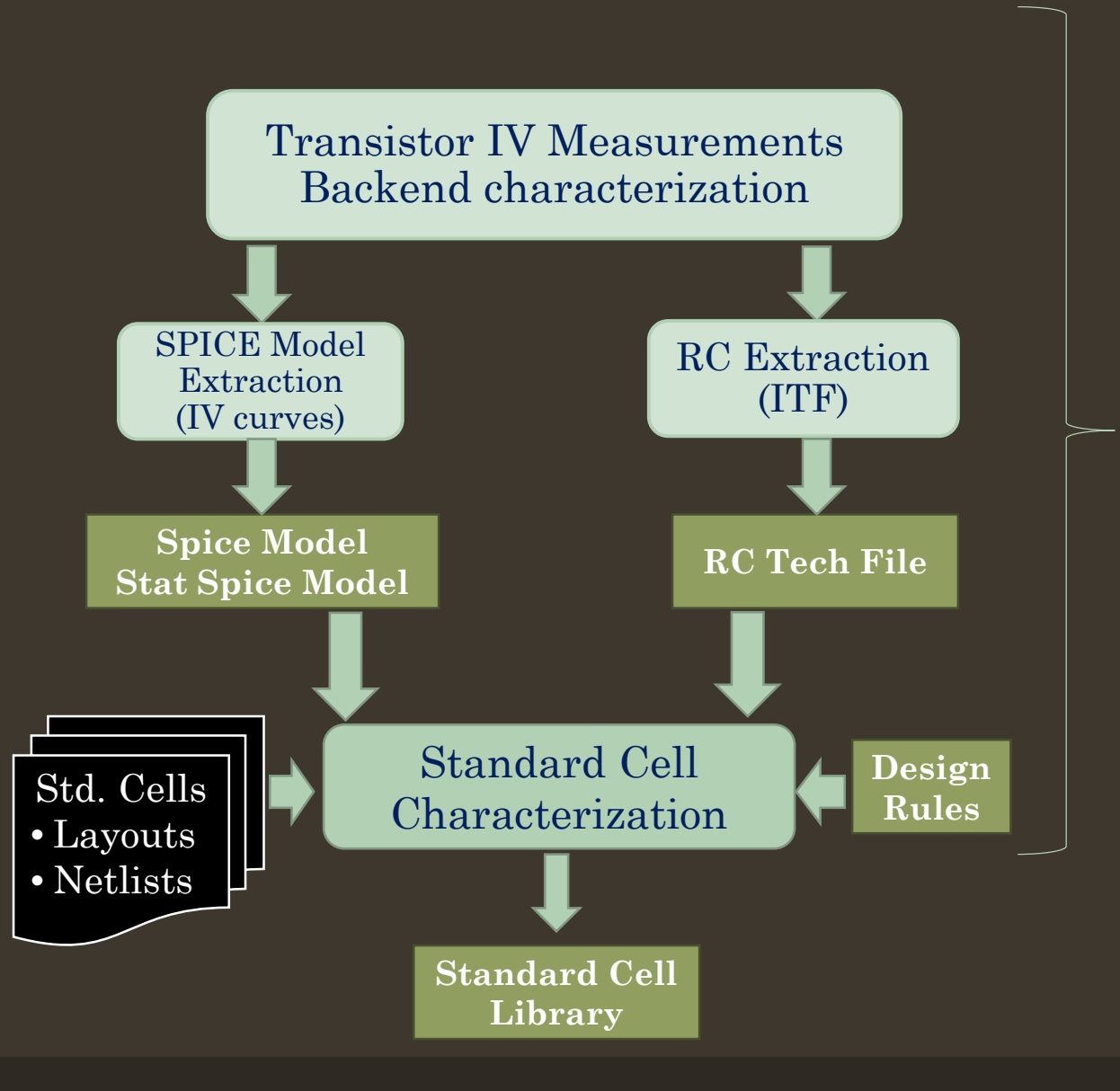
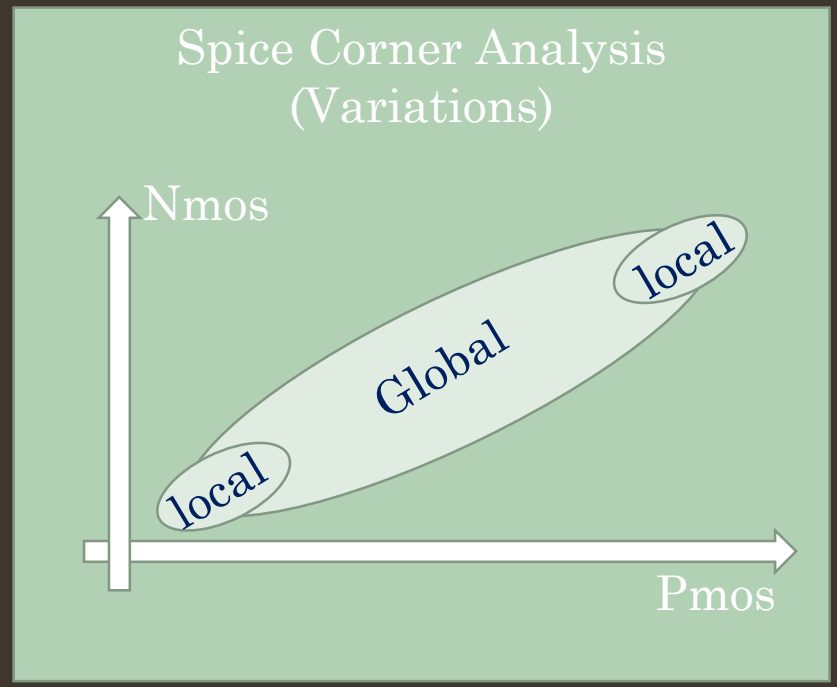
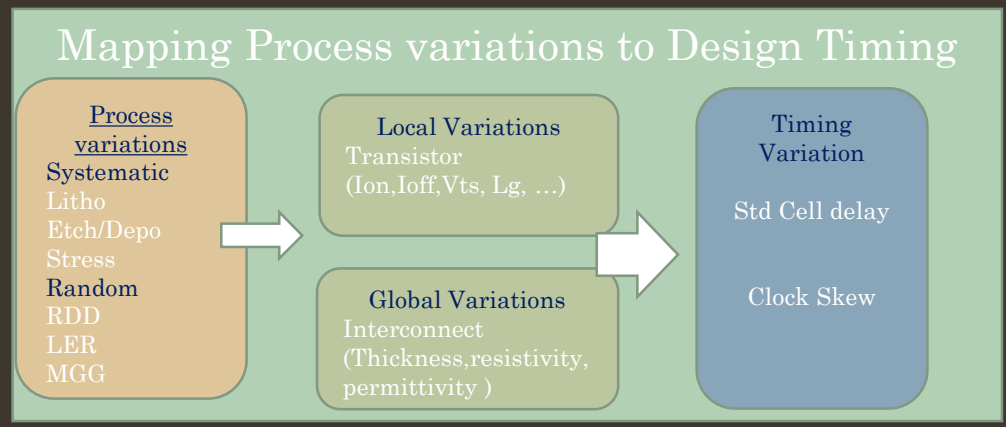
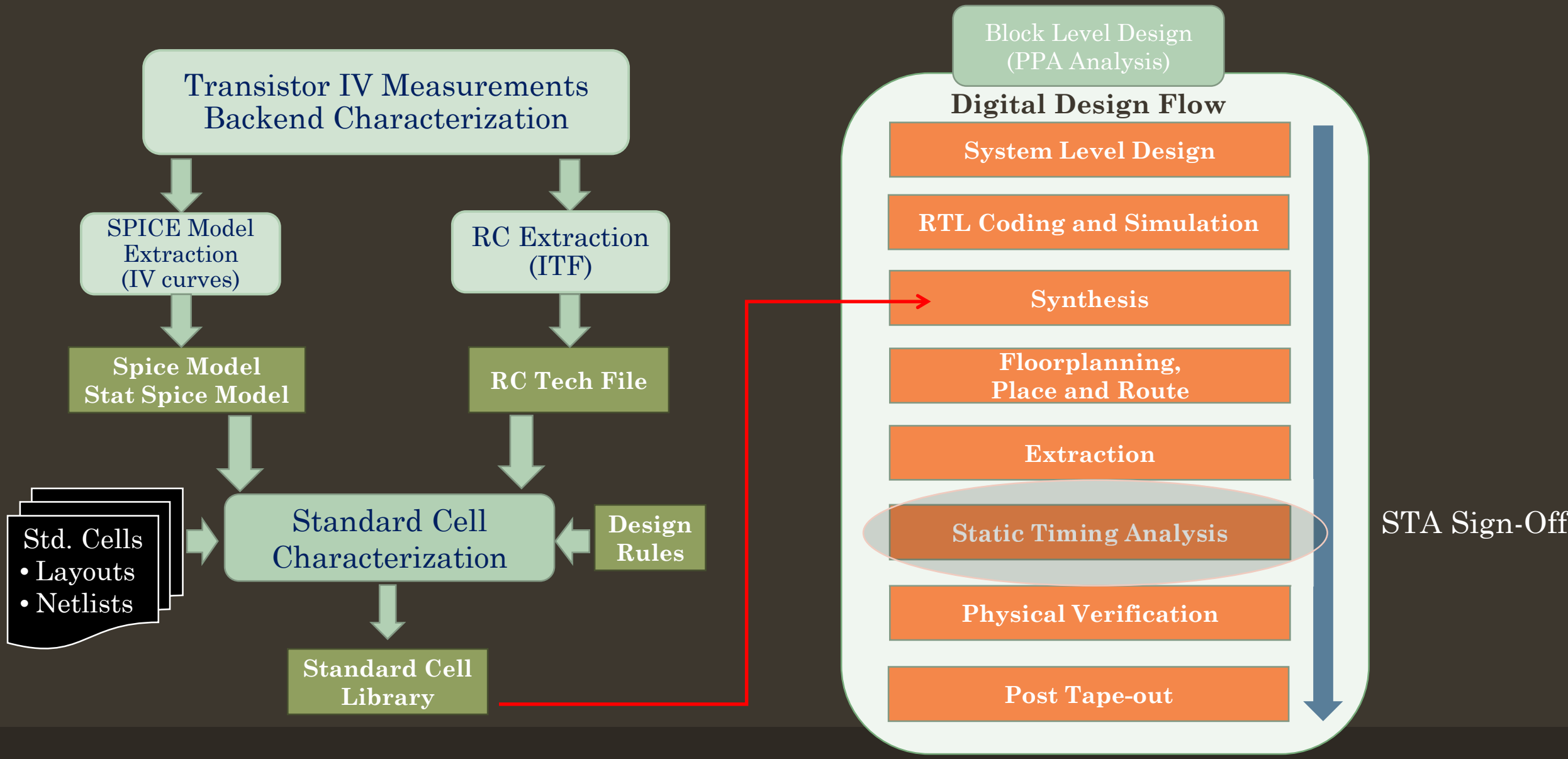
EDA DTCO FLOW : current flow based on Silicon and PDK (Standard Cell Characterization)







EDA DTCO FLOW : current flow with Digital Design Flow (Block Level)



TCAD DTCO FLOW : Alternative Flow before Silicon & PDK

(Standard Cell)

TCAD Transistor & Backend simulation

Spice Model
Stat Spice Model

RC Spice Netlist
Transistor netlist

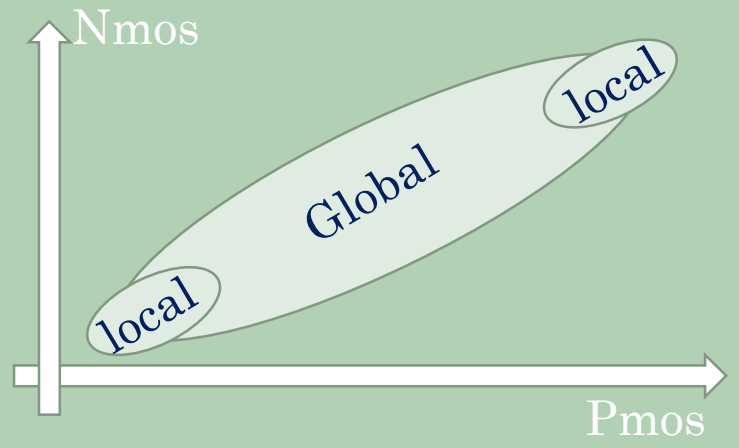
Transistor level Simulation and Standard Cell Characterization

Standard Cell Library

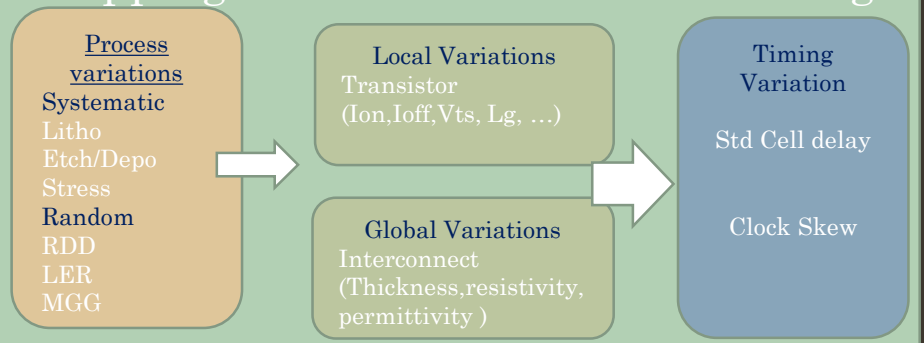
Flow made available by 3 TCAD companies (SNPS – Silvaco – GTS)

Std. Cell library made from TCAD (technically doable and still on-going work)

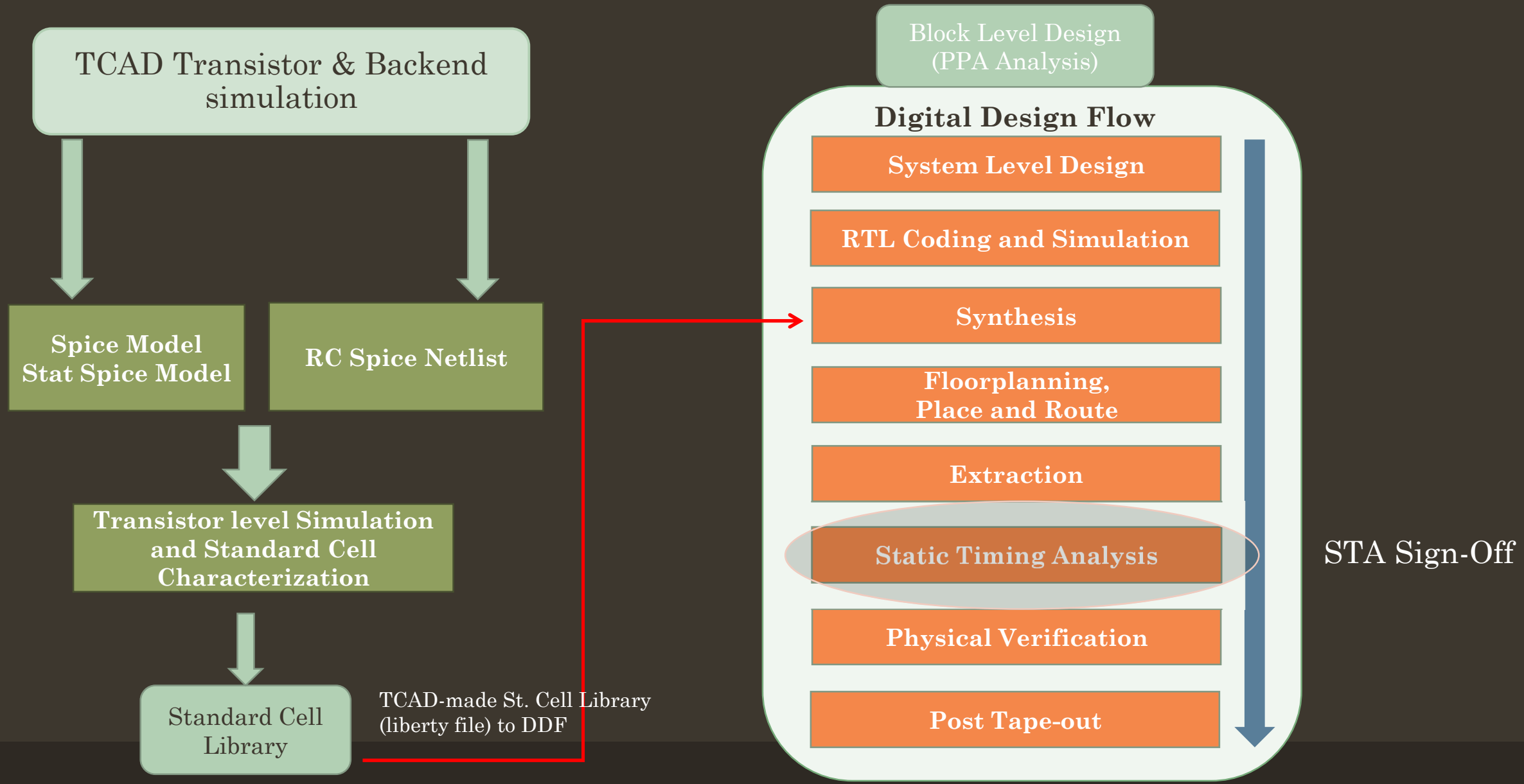
Spice Corner Analysis (Variations)



Mapping Process variations to Timing



TCAD DTCO FLOW : TCAD based Flow and Digital Design Flow (DDF)
No impact on DDF – output can be used seamlessly by Design Teams



TCAD/EDA DTCO FLOW Future : High Level Overview
Full integration from TCAD to Digital Design Flow (DDF)

Timing & Performance OK
(STA Sign-Off)

RTL

Synthesis

Timing Constraints

Gate-Level

Path Constraints

Place & Route

Parasitic Back
Annotation

Chip Layout

Design Sign-Off

Timing
Reports

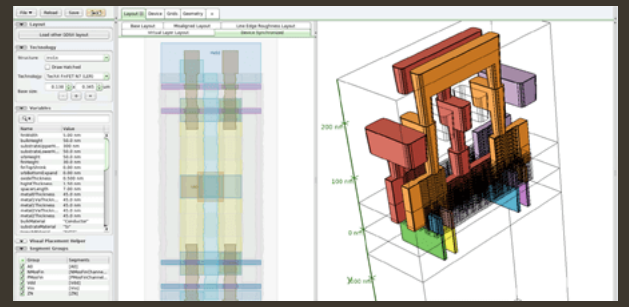
Performance
Power/Area
Yield/Cost

XTor/PEX New
Design

Specs not met

New Layout
(DR)

TCAD Flow
Device / Backend simulation
(Process - Device – Layout - PE)



TCAD
Standard

DTCO
Cell PPA

Gate Level Netlist

Static Timing Analysis

Design
Constraints

Cell Library
Timing Models

To EDA DDF

Spice & PEX
Models

Library characterization

TCAD to EDA

Cell Library
(Liberty .lib)